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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Charles W. Mitchell et al.
Title:	METHOD AND APPARATUS FOR USING AN ON-BOARD TEMPERATURE SENSOR ON AN INTEGRATED CIRCUIT

Application No.:	09/660,209	Filed:	September 12, 2000
Examiner:	Tung S. Lau	Group Art Unit:	2863
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APPELLANTS' BRIEF (37 C.F.R. § 1.192)

This brief is in furtherance of the Notice of Appeal, filed on June 11, 2004. The fees required under § 1.17(c), are provided in the accompanying Transmittal. This brief is being transmitted in triplicate pursuant to 37 C.F.R. § 1.192(a). As the two month period from the date of receipt of the Notice of Appeal was August 11, 2004, a petition for a one month extension of time accompanies this brief to extend the time period for filing to September 11, 2004.

REAL PARTY IN INTEREST

The real party in interest in this appeal is Advanced Micro Devices, Inc., as evidenced by the assignment recorded at Reel/Frame 011226/0469.

RELATED APPEALS AND INTERFERENCES

Appellants have no knowledge of any related appeals or interferences.

STATUS OF CLAIMS

Claims 1, 3 – 5, 7 – 13, 15, 18, 20 – 30, and 32 – 37 are presented herein on appeal. Claims 1 – 29 were originally presented. Claims 8, 13, 15, 20, 21, and 23 were amended, and

claims 14, 16, 17, and 19 were cancelled in a response filed March 31, 2003. Claims 18 and 25 were amended in a response filed on August 18, 2003, but those amendments were not entered. The same amendments to claims 18 and 25 were submitted and entered in a submission to support a request for continued examination filed October 17, 2003. The submission also added new claims 30 – 37. In a response filed on February 12, 2004, claims 1, 3 – 6, 8, 30, 32, and 33 were amended and claims 2 and 31 were cancelled. Claim 6 does not stand rejected, but has been objected to for being dependent on a rejected base claim.

Claims 1, 3 – 5, 7 – 13, 15, 18, 20 – 30, and 32 – 37 are now presented herein on appeal are reproduced in the Appendix attached hereto.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action mailed April 23, 2004.

SUMMARY OF INVENTION

An integrated circuit asserts a temperature control signal on at least one output terminal of the integrated circuit, based on a comparison of a temperature indicated by a temperature sensor of the integrated circuit and at least one temperature limit (page 4, first paragraph, lines 1 – 4, Figure 1). The signals asserted on the output terminal indicate that a system action should be taken, such as activating or deactivating a cooling device (page 4, first paragraph, lines 4 – 6, Figures 1 and 4). The integrated circuit may store multiple temperature limits, such as a high limit and a low limit (page 4, second paragraph, lines 5 – 11, Figure 2). The integrated circuit also deasserts signals on an output terminal based on comparison of an indicated temperature and one or more temperature limits or writing of a control bit (page 5, lines 19 – 25; page 6, lines 11 – 13). Furthermore, the output terminal can operate in a thermostat mode or an interrupt mode (page 5, lines 10 – 25).

ISSUES

The Issue on Appeal is whether Appellants' claims 1, 3 – 5, 7 – 13, 15, 18, 20 – 30, and 32 – 37 are anticipated by U.S. Patent No. 6,131,073 issued to Honda.

GROUPING OF CLAIMS

Appealed claims do not stand or fall together. The claims are grouped as follows:

Claims Group I: claims 1, 7 – 12

Claims Group II: claim 3, 32, 34

Claims Group III: claims 4, 20, 24

Claims Group IV: claims 5, 13

Claims Group V: claims 27, 28, 29

Claims Group VI: claims 23, 25

Claims Group VII: claims 15, 18

Claims Groups VIII: claim 21, 22

Claims Groups IX: claim 26

Claims Group X: claims 30, 33, 35, 36, 37

ARGUMENTS

Claims 1, 3 – 5, 7 – 13, 15, 18, 20 – 30, and 32 – 37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Honda. Anticipation under 35 U.S.C. § 102(e) requires that each and every element of the claim be taught in the reference. ATD Corp. v. Lydall Inc., 159 F.3d 534, 545, 48 USPQ2d 1321, 1328 (Fed. Cir. 1998). "An anticipating reference must describe the patented subject matter with sufficient clarity and detail to establish that its existence was recognized by person of ordinary skill in the field of the invention. Id. Anticipation requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Honda fails to disclose each and every element of the claims, expressly or inherently, as explained below, hence Applicant requests reversal of the rejections as to all claims.

Group I

Group I includes claims 1 and, 7 – 12. With regard to claim 1, the only independent claim of Group I, the final Office Action asserts that Honda teaches at col. 11, lines 19-48 and fig. 6 units 210-260 *an integrated circuit that asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value.* In the Response to Arguments the final Office Action also refers to col. 4, line 51 – col. 5, line 8, and col. 11, lines 19 – 47 to support the assertion that Honda discloses "asserting a temperature control signal and supplying the asserted signal on an output terminal of the integrated circuit" (page 8, final Office Action dated April 23, 2004). Honda teaches at col. 4, line 65 – col. 5, line 3 that:

> terminals Ta connected to an external EEPROM 30 which stores actuation data necessary for controlling the operating characteristics of the power source circuit 10. Under the control based on these actuation data, a constant power voltage V_{DD2} is always supplied from the power source circuit 10.

While terminal Ta is an output terminal, it fails to teach the claimed first output terminal of the integrated circuit. Ta is utilized for EEPROM access, not to supply a temperature control signal. At col. 11, lines 19-47, Honda teaches:

> More specifically, the threshold voltage of the MOS FET varies largely depending on a manufacturing process of an IC substrate (wafer) constituting this MOS FET. However, the temperature characteristics is derived from the physical properties of the semiconductor and therefore kept constant. For example, a measurement of the detection voltage is done beforehand at a room temperature. The detected value is written in EEPROM 30 as an initial value. When the semiconductor integrated circuit 2 is in use, a detection signal obtained from the temperature sensor 12 is compared with the initial value stored in EEPROM 30. A voltage difference thus obtained is then divided by the temperature characteristics (several mV/°C) relevant to the detection voltage, to obtain a temperature change or deviation from the room temperature.
>
> The above-described semiconductor integrated circuit 2 performs an initial setting processing for storing actuation data to EEPROM 20 as well as a control processing for correcting the output characteristics of the power source circuit 10 based on the actuation data stored in EEPROM 30 during an operation of the semiconductor integrated circuit 2.
>
> As shown in the flowchart of FIG. 5, the initial setting processing is executed in

> response to a mode switching command that is entered from the terminal Tb to change the operating mode of semiconductor integrated circuit 2 from an ordinary mode to an adjusting mode. CPU 20 reads a control program from the program memory 22 for executing this processing.

That portion of Honda describes obtaining a temperature deviation from room temperature, which is subsequently utilized ensure that a constant power voltage V_{DD2} is always supplied from the power source circuit. But that fails to teach asserting a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value. Honda instead teaches at col 7, lines 7-14 that "[o]nce the actuation data are completely written into the control register 38, the actuation circuit 42 flexibly closes one of analog switches SW1 – SW5 in accordance with the actuation data." The flexible closing of switches by the actuation circuit maintains a constant power voltage V_{DD2}. Thus, it can be seen from Honda's disclosure that the actuation data is not a temperature control signal.

The Office also refers to blocks 210 -260 to support rejection of claim 1. However, these control processing steps disclose the following:

```
210 - READ DETECTION VOLTAGE OF TEMP. SENSOR
220 - READ DATA FROM EEPROM
230 - CALCULATE TEMP. CHANGE ΔT
240 - CORRECT ACTUATION DATA
250 - WRITE CORRECTED ACTUATION DATA INTO CONTROL REGISTER
260 - EXECUTE METER CONTROL PROCESSING
```

None of these steps teach or suggest asserting a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value as recited in claim 1. Instead, that portion of Honda teaches ensuring that voltage output is constant, utilizing temperature change data determined by comparing a current temperature measurement to stored data in the EEPROM to determine the change in temperature and thus the correction needed to maintain the voltage constant.

As pointed out in MPEP 2131, "[a] claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that Honda fails to teach at least *an*

integrated circuit that asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value.

In view of the above remarks, Applicants respectfully submit that the rejection of claims 1, 7 – 12 under 35 U.S.C. §102(e) should be reversed.

Group II

Group II includes claims 3, 32, and 34. Claim 3 recites that *the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value.* The final Office Action argues that Honda discloses "deassert[ing] the signals in response to temperature changes according to [a] mode of operation" and cites col. 2, lines 30 – 55 and Figure 2 unit 42 as support for the rejection. Honda discloses "a terminal for outputting the direct-current constant voltage and a terminal for adjusting the actuating circuit" (col. 2, lines 30 – 34). Unit 42 of Figure 2 is an actuation circuit described by Honda as follows at col. 7, lines 7 – 14:

> The actuation circuit 42 forcibly closes the analog switch SW3 for a predetermined duration immediately after the semiconductor integrated circuit 2 is activated until the actuation data are written into the control register 38. Once the actuation data are completely written into the control register 38, the actuation circuit 42 flexibly closes one of analog switches SW1 – SW5 in accordance with the actuation data.

Honda discloses at col. 2, lines 34-55:

> a temperature sensor detecting a temperature of the electronic circuit. The actuation data are corrected based on the temperature detected by the temperature sensor and the adjusting circuit is actuated based on the corrected actuation data, so as to eliminate undesirable temperature drift in the operating parameters of the electronic circuit.
>
> .
> .
> .

> Preferably, the memory means stores temperature data sensed by the temperature sensor at a time the actuation data are set, in addition to the actuation data. And, the control means corrects the actuation data based on the temperature data memorized in the memory means and a present temperature sensed by the temperature sensor.

This section of Honda is devoid of any disclosure or suggestion of an integrated circuit deasserting a temperature control signal, much less deasserting when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value, as recited in claim 3.

In the Response to Arguments section of the Final Office Action, the Office again refers to col. 11, lines 19 – 47 and col. 4, line 51 – col. 5, line 7 as support for rejection of claim 3. As already stated above Honda fails to disclose or teach asserting a signal on an integrated circuit's output terminal as claimed. Thus, Honda cannot teach deasserting the signal on the output terminal.

Accordingly, applicant respectfully submits that Honda fails to anticipate claim 3 or any of the claims in group II and thus the rejection of claims 3, 32, and 34 under 35 U.S.C. §102(e) should be reversed.

Group III

Group III includes claims 4, 20, and 24. Claim 4 recites that *the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, in response to access to a control location in the integrated circuit.* Claim 20 recites *accessing a control location in the integrated circuit to cause the signal to be deasserted.* Claim 24 recites that *the second signal is deasserted by accessing a control location in the integrated circuit.* With regard to claim 20, the Office Action relies on col. 2, line 56 to col. 3 line 19 and Figs 1 and 2 as teaching accessing a control location in the intergrated circuit to cause the signal to be deasserted. The final Office Action also asserts that Honda discloses "accessing a control location in an IC to deassert a signal on an output terminal" at col. 11 lines 19-47, and col. 4, line 51-col. 7. Figure 1 is a schematic block diagram of an integrated circuit and includes I/O block 26 that inputs a detection signal from a vehicle speed sensor and outputs a control signal to an external actuation circuit. However there is no signal, corresponding to

claimed signal (generated by a comparison of the measured temperature to a first limit value) that is deasserted in response to access to a control location. Figure 2 depicts a circuit diagram of a power source circuit. Neither these Figures nor their accompanying descriptions, nor does Honda teach or suggest elsewhere, *accessing a control location in the integrated circuit to cause the signal to be deasserted.*

Accordingly, Applicants respectfully submit that the rejection of claims 4, 20, and 24 under 35 U.S.C. §102(e) should be reversed.

Group IV

Group IV includes claims 5 and 13. *Claim 13 recites the signal on the first output terminal is deasserted in response to either a control location on the integrated circuit being accessed or the measured temperature falling below a lower limit value, <u>according to a programmable mode of operation</u>.* The final Office Action asserts that is taught at col. 2, line 50 to col. 3, line 19. The Office Action also refers to unit 22 of Figure 1. Unit 22 of Figure 1 is program memory. The program memory 22 does not disclose the limitation of claim 13 noted above. Honda fails to disclose deasserting a temperature control signal, whether in response to a measured temperature falling below a lower temperature limit or in response to a control location being accessed. Further, there is no teaching anywhere regarding <u>a programmable mode of operation</u> that determines how deassertion occurs.

For at least these reasons, Applicants respectfully submit that the rejection of claims 5 and 13 under 35 U.S.C. §102(e) should be reversed.

Group V

Group V includes claims 27, 28, and 29. Claim 27 is the sole independent claim of Group V and recites a microprocessor that comprises *compare logic coupled to the temperature sensor and to the programmable storage locations storing the first and second temperature limit values, <u>to provide respectively a first and second signal indicative of a comparison between the temperature measurement and the first and second temperature limit values</u>; and <u>first and second output terminals coupled to provide respectively, the first and second signals</u>*. The final Office Action relies on col. 2, lines 35-55 as teaching a first and second signals and col. 2, line

35 to col. 3, line 3 and Fig. 2 as teaching the first and second output terminals. Fig. 2 shows control signal from the actuation circuit but fails to teach the claimed first and second output terminals.

For at least these reasons, Applicants respectfully submit that the rejection of claims 27 and 29 under 35 U.S.C. §102(e) should be reversed.

Group VI

Group VI includes claims 23 and 25. Applicants respectfully submit that Honda fails to disclose or suggest *asserting a second signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby* <u>*indicating that the temperature has exceeded a safe limit*</u> as recited in claim 23. The Final Office Action refers to col. 2, lines 30 – 55, which discloses correcting actuation data based on an initial temperature measurement and a current temperature measurement. Honda does not disclose or teach indicating that the temperature of the integrated circuit has exceeded safe limit, at least because Honda discloses maintaining a constant power voltage, and not indicating whether the temperature of an integrated circuit has exceeded a safe limit. Nothing can be found within Honda that teaches or suggests such indication of exceeding a safe limit or asserting a second output terminal of the integrated circuit when the measured temperature is above the second limit value.

The Final Office Action also relies on Figure 6 to support rejection of claim 23. The Final Office Action specifically refers to blocks 210 – 260 of Figure 6. These blocks are as follows:

```
210 - READ DETECTION VOLTAGE OF TEMP. SENSOR
220 - READ DATA FROM EEPROM
230 - CALCULATE TEMP. CHANGE ΔT
240 - CORRECT ACTUATION DATA
250 - WRITE CORRECTED ACTUATION DATA INTO CONTROL REGISTER
260 - EXECUTE METER CONTROL PROCESSING
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Nothing can be found in these blocks, or anywhere else in Honda, that discloses a safe limit or asserting a second output terminal of the integrated circuit when the measured temperature is above the second limit value.

For at least these reasons, Applicants respectfully submit that the rejection of claims 23 and 25 under 35 U.S.C. §102(e) should be reversed.

Group VII

Groups VII includes claims 15 and 18. With regard to claim 15, the Final Office Action relies on col. 1, line 50 – col. 2, line 30, which discloses correcting actuation data to control voltage supplied to an electronic circuit. Nothing can be found in Honda that discloses or suggests asserting a signal to inhibit a cooling device as recited in claim 15, or asserting a signal to directly control a cooling device as recited in claim 18. The section cited by the Final Office Action lists numerous components of Honda's circuit, but controlling or inhibiting a cooling device cannot be found anywhere within Honda.

For at least these reasons, Applicants respectfully submit that the rejection of claims 15 and 18 under 35 U.S.C. §102(e) should be reversed.

Group VIII

Group VIII includes claim 21 and claim 22, which depends on claim 21. Applicants respectfully submit that Honda fails to teach that *the asserted signal causes an assertion of an interrupt and wherein a sequence of instructions, responsive to the asserted interrupt, activates a cooling device*. The final Office Action seems to reject claim 21 by stating "a control location in the IC, including at least one cooling device in response to asserted signal" and refers to unit 42 of Figure 2. Unit 42 of Figure 2 is the actuation circuit, previously discussed. Honda fails to teach anything regarding a cooling device. The Final Office Action fails to address where Honda teaches an assertion of an interrupt or activation of a cooling device.

For at least these reasons, Applicants respectfully submit that the rejection of claim 21 under 35 U.S.C. §102(e) should be reversed.

Group IX

Group IX includes only claim 26. Claim 26 recites a computer system that comprises at least one cooling device, which activates in response to an asserted signal on at least one of the two output terminals. As already discussed, Honda does not disclose or suggest asserting a

signal to activate a cooling device. Honda especially does not disclose a computer system with a cooling device. Nothing in the Figures nor the disclosure of Honda can be found that discloses or suggest a cooling device.

For at least these reasons, Applicants respectfully submit that the rejection of claim 26 under 35 U.S.C. §102(e) should be reversed.

Group X

Group X includes claims 30, 33, 35, 36, and 37. With regard to claim 30, the sole independent claim of the Group, the final Office Action argues that Honda discloses all limitations of claim 30, and in particular "a first output coupled to provide a first temperature control signal corresponding to the indication provided by the compare logic". In the Response to Arguments the final Office Action also refers to col. 4, line 51 – col. 5, line 8, and col. 11, lines 19 – 47 to support the assertion that Honda discloses "asserting a temperature control signal and supplying the asserted signal on an output terminal of the integrated circuit" (page 8, Final Office Action dated April 23, 2004). Honda teaches at col. 4, line 65 – col. 5, line 3) that:

> terminals Ta connected to an external EEPROM 30 which stores actuation data necessary for controlling the operating characteristics of the power source circuit 10. Under the control based on these actuation data, a constant power voltage V_{DD2} is always supplied from the power source circuit 10.

The final Office Action presumably considers the terminal Ta as corresponding to the claimed first output. However, Honda fails to disclose outputting a temperature control signal over terminal Ta. The relied upon sections disclose outputting to the EEPROM initial actuation data and an initial temperature indication, and providing corrected actuation data to the EEPROM, without any teaching of providing a temperature control signal to the EEPROM. Honda instead teaches at col 7, lines 7-14 that "[o]nce the actuation data are completely written into the control register 38, the actuation circuit 42 flexibly closes one of analog switches SW1 – SW5 in accordance with the actuation data." The flexible closing of switches by the actuation circuit maintains a constant power voltage V_{DD2}. Thus, it can be seen from Honda's disclosure that the actuation data is not a temperature control signal. Furthermore, Honda teaches no reason to provide a temperature control signal to an EEPROM. The EEPROM stores data, such as the

actuation data as disclosed in Honda. There is no disclosure or suggestion in Honda for supplying a temperature control signal to the EEPROM.

As pointed out in MPEP 2131, "[a] claim is anticipated only if each and every element as set forth in the claims is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that Honda fails to teach at least *a first output coupled to provide a temperature control signal corresponding to the indication provided by the compare logic.*

In view of the above remarks, Applicants respectfully submit that the rejection of claims 30, 33, 35, 36, and 37 under 35 U.S.C. §102(e) should be reversed.

CONCLUSION

For at least the foregoing reasons, applicants respectfully submit that the claims on appeal are not anticipated by Honda. Accordingly, the Board is respectfully requested to reverse the rejection of claims 1, 3 – 13, 15, 18, 20 – 30, and 32 – 37.

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

1. An integrated circuit comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

a programmable storage location storing a first temperature limit value, the programmable storage location accessible via an instruction executed by the integrated circuit; and

compare logic coupled to the temperature sensor and the storage location to provide an indication of a comparison between the temperature measurement and the first temperature limit value, wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement is above the first temperature limit value.

3. The integrated circuit as recited in claim 1 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement indicated by the temperature sensor falls below a programmable second temperature limit value.

4. The integrated circuit as recited in claim 1 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, in response to access to a control location in the integrated circuit.

5. The integrated circuit as recited in claim 1 wherein the integrated circuit deasserts the first temperature control signal, which is supplied on the first output terminal of the integrated circuit, when the temperature measurement falls below a programmable second temperature limit

value or when a control location in the integrated circuit is accessed, according to a programmable mode of operation.

6. The integrated circuit as recited in claim 1 wherein the first temperature limit value is a panic value indicating a temperature limit for safe integrated circuit operation.

7. The integrated circuit as recited in claim 1 further comprising an addressable storage location coupled to the temperature sensor, the addressable storage location accessible by an instruction executed by the integrated circuit and supplying an indication of the temperature measurement on the integrated circuit.

8. The integrated circuit as recited in claim 1 further comprising:

a second output terminal coupled to provide external to the integrated circuit an asserted signal when the temperature measurement indicated by the temperature sensor is above a second temperature limit value.

9. The integrated circuit as recited in claim 8 further comprising:

a second storage location supplying the second temperature limit value; and

second compare logic coupled to the second storage location and coupled to receive the temperature measurement of the integrated circuit, and wherein the second compare logic generates a second indication of when the temperature measurement of the integrated circuit is above the second temperature limit value.

10. The integrated circuit as recited in claim 9 further comprising:

a third storage location supplying a third temperature limit value;

third compare logic coupled to the third storage location and coupled to receive the temperature measurement, and wherein the compare logic generates a third indication that the temperature measurement of the integrated circuit is below the third temperature limit value.

11. The integrated circuit as recited in claim 10 wherein the integrated circuit asserts a first temperature control signal which is supplied on a first output terminal of the integrated circuit when the temperature measurement indicated by the temperature sensor is below the third temperature limit value.

12. The integrated circuit as recited in claim 1 wherein the integrated circuit is a microprocessor.

13. A method comprising:

measuring a temperature of an integrated circuit with a temperature sensor, the temperature sensor being a circuit within the integrated circuit;

comparing the measured temperature to a first limit value stored in the integrated circuit; and

generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit, wherein

the signal is asserted when the measured temperature is greater than the first limit value, and wherein

the signal on the first output terminal is deasserted in response to either a control location on the integrated circuit being accessed or the measured temperature falling below a lower limit value, according to a programmable mode of operation.

15. The method as recited in claim 13 wherein the asserted signal is used to inhibit a cooling device to control the temperature of the integrated circuit.

18. The method as recited in claim 13 wherein the signal is utilized to directly control a cooling device.

20. A method comprising:

measuring a temperature of an integrated circuit with a temperature sensor, the temperature sensor being a circuit within the integrated circuit;

comparing the measured temperature to a first limit value stored in the integrated circuit;

generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit; and

accessing a control location in the integrated circuit to cause the signal to be deasserted.

21. The method as recited in claim 13 wherein the asserted signal causes assertion of an interrupt and wherein a sequence of instructions, responsive to the asserted interrupt, activates a cooling device.

22. The method as recited in claim 21 wherein an instruction sequence causes the signal to be deasserted.

23. A method comprising:

measuring a temperature of an integrated circuit with a temperature sensor, the temperature sensor being a circuit within the integrated circuit;

comparing the measured temperature to a first limit value stored in the integrated circuit; and

generating a signal on a first output terminal of the integrated circuit according to the comparison to control the temperature of the integrated circuit;

comparing the measured temperature to a second limit value stored in the integrated circuit; and

asserting a second signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that temperature has exceeded a safe limit.

24. The method as recited in claim 23 wherein the second signal is deasserted by accessing a control location in the integrated circuit.

25. An apparatus comprising:

a processor including,

means for measuring a_temperature of the processor-and providing a measured temperature;

means for comparing the measured temperature to at least a first limit value and a second limit value;

means for providing a control signal on a first output terminal of the processor according to the comparison of the measured temperature to the first limit value, the control signal to control the temperature of the integrated circuit; and

means for providing an indicator signal on a second output terminal of the integrated circuit when the measured temperature is above the second limit value, thereby indicating that the measured temperature has exceeded a safe limit.

26. The apparatus as recited in claim 25 wherein the apparatus is a computer system and further comprises at least one cooling device, which activates in response to an asserted signal on at least one of the two output terminals.

27. A microprocessor comprising:

a temperature sensor providing a temperature measurement of the integrated circuit;

at least a first and second temperature limit value stored in programmable storage locations in the microprocessor, the storage locations being accessible via software executed by the microprocessor;

compare logic coupled to the temperature sensor and to the programmable storage locations storing the first and second temperature limit values, to provide respectively a first and second signal indicative of a comparison between the temperature measurement and the first and second temperature limit values; and

first and second output terminals coupled to provide respectively, the first and second signals.

28. The microprocessor as recited in claim 27 wherein the microprocessor deasserts the first signal, which is supplied on the first output terminal of processor, when the temperature measurement falls below a programmable third temperature limit value, thereby providing a thermostat mode of operation for the first signal.

29. The integrated circuit as recited in claim 27 wherein the microprocessor includes a software accessible control register controlling operation of the compare logic and the first and second output terminals.

30. An integrated circuit comprising:

a temperature sensor to provide a measured temperature of the integrated circuit;

a storage location to hold a first programmable value indicating a first temperature limit;

compare logic coupled to compare the measure temperature and the first temperature limit and to provide an indication of the comparison; and

a first output coupled to provide a first temperature control signal corresponding to the indication provided by the compare logic.

32. The integrated circuit as recited in claim 30 wherein the first temperature control signal is asserted in response to an indication that the measured temperature exceeds the first temperature limit, and wherein the first temperature control signal is deasserted in response to an indication that the measured temperature does not exceed the first temperature limit.

33. The integrated circuit as recited in claim 30 further including a second storage location to hold a second programmable value indicating a second temperature limit, and wherein the compare logic is further to compare the measured temperature and the second temperature limit and to provide a second indication thereof.

34. The integrated circuit as recited in claim 33 wherein the first temperature control signal is asserted in response to an indication that the measured temperature exceeds the first temperature limit, and wherein the first temperature control signal is deasserted in response to

the second indication that the measured temperature does not exceed the second temperature limit.

35. The integrated circuit as recited in claim 33, further comprising a second output coupled to provide an indicator signal in response to the second indication provided by the compare logic, wherein the indicator signal indicates that the integrated circuit has exceeded the second temperature limit.

36. The integrated circuit as recited in claim 33 further comprising a third storage location to hold a control value, and wherein a state of the first temperature control signal is controlled, at least in part by the control value.

37. The integrated circuit as recited in claim 36, wherein the first temperature control signal is asserted in response to an indication that the measured temperature exceeds the first temperature limit, and wherein the first temperature control signal is deasserted in response to the control value.